

Serial No.: 09/539,637

Attorney's Docket No.: 10559/170001/P8263

REMARKS

In view of the foregoing amendments and the following remarks, reconsideration and allowance are respectfully requested.

Claims 1-21 and 23 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Pannell (US Patent 5,808,630) in view of Chee (US Patent 5,694,141). This contention is respectfully traversed.

Claims 1-3, 8, 10-11, 14-20, 23 have been amended, with Claims 1, 2, 8, 10, 14, 17, 18 and 23 being independent. No new matter has been added.

Claim 1

Claim 1 is patentable over Pannell and Chee at least because the cited references in the combination suggested by the office action fail to teach or suggest each and every feature of the claim. For example, the cited references, alone or in combination, fail to teach or suggest "utilizing a video memory bandwidth twice for each full line of video overlay data stored in the line buffer."

For example, Pannell discloses a split video architecture to merge video data into a composite frame buffer with desktop data (Pannell: Abstract). However, as acknowledged on page 2 of the office action, "Pannell does not disclose setting an indicator in a line buffer, determining when the pixel data reaches the indicator; and loading data for the next video line into the buffer based on the determining when the pixel data reaches the indicator, wherein the indicator is at approximately a middle of the line buffer." Therefore, Pannell fails to teach several features of Claim 1.

Serial No.: 09/539,637

Attorney's Docket No.: 10559/170001/P8263

Chee fails to remedy the deficiencies of Pannell because Chee fails to teach or suggest each and every feature of Claim 1. Chee discloses a computer system with a video display controller (VDC) to decode data words from a first bit-word format as received from a display first-in-first-out (FIFO) memory to a second bit-word format as required by one of a pair of display devices (Chee: Abstract). Chee discloses a FIFO-LO indicator and a FIFO-HI indicator to determine a memory fetch priority to a memory arbiter (Chee: Col. 6, lines 53-59; Col. 11, lines 1-47). The FIFO-LO indicator is for a FIFO issuing a request for access to a DRAM on a low priority basis, and the FIFO-HI indicator is for the FIFO issuing a request for access to a DRAM on a high priority basis (Chee: Col. 6, lines 53-59).

However, Chee's use of the indicator differs from Claim 1. Instead, Claim 1 recites:

utilizing a video memory bandwidth twice for each full line of video overlay data stored in the line buffer, wherein the utilizing the video memory bandwidth twice comprises:

*setting an indicator in a line buffer,
the line buffer to store up to the full line
of video overlay data for the overlay
window;*

*reading pixel data for a current video
line from the line buffer;*

*determining when the pixel data reaches
the indicator;*

*loading pixel data for a first half of
a next video line into the line buffer based
on the determining when the pixel data for
the current video line reaches the
indicator, wherein the indicator is at*

Serial No.: 09/539,637

Attorney's Docket No.: 10559/170001/P8263

approximately a middle of the line buffer;
and

loading pixel data for a second half of
the next video line into the line buffer
based on determining when the line buffer is
about empty of the current video line of
pixel data (emphasis added).

Because the memory system can allocate bandwidth to other request agents while outside of the time slots at the middle and end of the display line, the memory system has the advantage of being used more efficiently by reducing the switching of request agents.

Furthermore, Claim 1 recites loading pixel data one half line at a time into the video line buffer. In contrast, Chee discloses loading pixel data at least one double-word level at a time (Chee: Col. 11, lines 13-16).

Also, the utilization of the video memory bandwidth as recited in Claim 1 provides advantages not disclosed in Chee or Pannell. For example, the horizontal blank time (Hblank) time requirement is reduced, which allows the technique of Claim 1 to be used with more advanced and higher resolution displays (Instant Disclosure: page 4, lines 5-11; page 2, lines 1-7).

The amendments to Claim 1 are supported in the specification and do not add new matter. For example, "to allow additional time to process the next overlay scan line 145 and therefore reduce the need to have increased memory bandwidth, the present invention uses the overlay display position locator 150" (Instant Disclosure: page 4, lines 12-15. See also, page 4, lines 5-11, 17-24; page 5, lines 1-6; page 2, lines 1-7).

For at least these reasons, the Applicants submit that Claim 1 is patentable over Chee and Pannell, and the rejection under 35 U.S.C. 103 should be respectfully withdrawn.

Serial No.: 09/539,637

Attorney's Docket No.: 10559/170001/P8263

Claims 2, 8, 10, 14, 18, and 23

Claims 2, 8, 10, 14, 18, and 23 recite subject matter similar to Claim 1 and are patentable for reasons similar to Claim 1.

These independent claims are also patentable for other recited subject matter. For example, Claim 2 recites "utilizing a video memory bandwidth twice for each full line of video overlay data stored in the line buffer to reduce a requirement for an amount of horizontal blanking (Hblank) time for a display monitor." Chee and Pannell fail to disclose the features of reducing a requirement for an amount of horizontal blanking time as recited in Claim 2. Chee and Pannell also fail to disclose utilizing the video memory bandwidth twice for each full line of video overlay data for the line buffer.

The recited subject matter above can avoid having the memory bandwidth being occupied by the overlay engine/pixel processing engine for an extended amount of time by fetching a full line of overlay scan line data consecutively. The efficiency of memory access can be increased by reducing the switching of request agents and by reducing the memory arbitration activity. The recited subject matter above also avoids having the memory bandwidth being occupied by the overlay engine/pixel processing engine by using the memory bandwidth continuously by fetching video data as soon as the FIFO is not full. The recited subject matter above allows the overlay engine/pixel processing engine to use the memory bandwidth twice for a certain amount of time by fetching half of the overlay scan line data in one display scan line at a time.

The recited subject matter in Claim 2 also provides additional advantages over Chee and Pannell. As mentioned above with respect to the advantages of Claim 1, by fetching a half

Serial No.: 09/539,637

Attorney's Docket No.:10559/170001/P8263

line of the next overlay scan line data during the active display time, the recited subject matter can allow support of a monitor with a reduced Hblank time requirement and also can allow a reduction of a requirement for a high memory bandwidth for a display.

For at least these reasons, the Applicants respectfully request that the 35 U.S.C. 103 rejections to independent Claims 2, 8, 10, 14, 18, and 23 be withdrawn.

Claims 3-7, 9, 11-13, 15-17, 19-21

Claims 3-7, 9, 11-13, 15-17, 19-21 are all patentable at least because these claims depend upon an allowable base claim (base Claim 1 for Claims 3-7; base Claim 8 for Claims 9, 11-13; base Claim 14 for Claims 15-17; and base Claim 18 for Claims 19-21). These dependent claims are also allowable for reciting patentable subject matter in their own right. The Applicants respectfully request that these dependent claims be put in condition for allowance.

Conclusion

In view of the remarks and amendments herein, Claims 1-21 and 23 are in condition for allowance and a notice to that effect is respectfully solicited. The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, Applicants' arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.


Serial No.: 09/539,637

Attorney's Docket No.:10559/170001/P8263

No fee is believed to be due at this time. Please apply
any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 08/03/05


Dwight U. Thompson
Reg. No. 53,688
Agent for Intel Corporation

Fish & Richardson P.C.
PTO Customer Number: 20985
12390 El Camino Real
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10517036.doc